Developments of Engineering Model of the X-ray CCD Camera of the MAXI Experiment onboard the International Space Station

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Abstract

MAXI, Monitor of All-sky X-ray Image, is an X-ray observatory on the Japanese Experimental Module (JEM) Exposed Facility (EF) on the International Space Station (ISS). MAXI is a slit scanning camera which consists of two kinds of X-ray detectors: one is a one-dimensional position-sensitive proportional counter with a total area of $\sim 5000 \text{ cm}^2$, the Gas Slit Camera (GSC), and the other is an X-ray CCD array with a total area $\sim 200 \text{ cm}^2$, the Solid-state Slit Camera (SSC). The GSC subtends a field of view with an angular dimension of $1^\circ \times 180^\circ$ while the SSC subtends a field of view with an angular dimension of $1^\circ$ times a little less than $180^\circ$. In the course of one station orbit, MAXI can scan almost the entire sky with a precision of $1^\circ$ and with an X-ray energy range of $0.5–30 \text{ keV}$.

We have developed an engineering model (EM) for all components of the SSC. Their performance test is ongoing. We have also developed several kinds of CCDs fabricated from different wafers. Since the thermal condition of the ISS is not suitable for the CCD operation, the operating temperature of the CCD estimated to be $-85 \sim -50^\circ\text{C}$ at the end of mission life. We therefore carefully need to choose CCD considering not only detection efficiency and readout noise but also the dark current. We report here the current status of the EM of the SSC and the X-ray responsivity of CCDs.

Key words: Charge-coupled device; X-ray detectors; International space station

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1 INTRODUCTION

Most recent X-ray satellites carry charge-coupled device (CCD) cameras for their focal plane instruments. The CCD possesses a moderate energy resolution, a high spatial resolution, and a timing resolution. The Solid-state Imaging Spectrometer, SIS, onboard ASCA is the first CCD camera used in space as a photon counting detector and equipped on board the satellite (Tanaka et al. 1994). Following the SIS, many satellites such as Chandra (Weisskopf et al. 1995), XMM-Newton (Barr et al. 1988), HETE2 (Ricker 1998) and MAXI (Matsuoka et al. 1997; Matsuoka et al. 1998) carry an X-ray CCD camera on their focal planes.

MAXI has been selected as an early payload of the JEM (Japanese Experiment Module) Exposed Facility on the International Space Station. MAXI will monitor activities of about 2000-3000 X-ray sources. It consists of two kinds of X-ray detectors: one is a one-dimensional position-sensitive proportional counter, the Gas Slit Camera (GSC), and the other is an X-ray CCD array, the Solid-state Slit Camera (SSC). CCDs, used for the SSC, are calibrated both at Osaka University and the National Space Development Agency of Japan (NASDA).

MAXI is now at the fabrication phase of the engineering model (EM). We here describe the EM of the SSC. The block diagram of SSC is shown in Figure 1. The SSC consists of four parts: camera assembly (SSCU), analog electronics (SSCE), digital processor (DP), and cooling system (SSCC).

2 Engineering Model of SSC

2.1 SSCU

The EM of SSCU is shown in Figure 2. MAXI carries Two SSCUs (SSC-H and SSC-Z). Each SSCU possesses 16 CCD chips. In this figure, we installed only three CCD chips and the collimator was removed. Details of CCDs are described later. In order to monitor a gain and a charge transfer efficiency, $^{55}$Fe source is installed in the SSCU.
There are several techniques of the CCD video signal processing (Janesick 2001). To measure the voltage of each charge packet, we need a reference voltage between the signal level and the float level. Note that the float level is the dc level of each pixel generated by the CCD and off-chip electronics. The correlated double sampling technique is widely used for this purpose. In practice, it is an advantageous point to integrate or take the sum of the signals rather than merely spot sample floating and signal levels. Thus, a delay-line circuit was employed in the ASCA SIS and an integrated circuit is introduced for the HETE SXC, the Chandra ACIS and the Astro-E XIS. We have developed these three circuits collaborating with Meisei Electric K.K for EM of SSCE and investigate their noise characteristics. We confirm that the integration circuit possesses the best noise performance. Therefore, we have decided to employ the integration circuit for the flight module as well as for the ground calibration.

The CCD video signal processed by the integration circuit is sampled by a 12-bit analog-digital converter (ADC). Digital data are transferred to the DP.

Since the data rate of CCDs is fairly high, an onboard data reduction system is inevitable. We developed an efficient reduction system based on our experiences with the ASCA SIS and the Astro-E XIS. There are three parts in DP: the control unit, the event handling unit (EHU), and the telemetry unit as shown in Figure 1. Two CPU boards having the RISC CPU of R3081 on the VME bus will be employed for EHU and other CPU boards will be used for the control unit, the telemetry unit, and the GSC data processing.

There are two interfaces between MAXI and JEM EF: medium-speed interface (10Base-T ethernet) and low-speed interface (MIL1553B). All CCD data and house-keeping (HK) data will be downlinked through the ethernet due to their large data size. Health and status (HS) data and HK data will be transferred through MIL1553B.

Based on the ASCA SIS, we have learned much about radiation damage on the CCD (Yamashita et al. 1997). One serious problem is an increase in dark current and its non-uniformity. To minimize the effects of radiation damage on the CCD, we allocate a bias level buffer for each pixel. The bias level for each pixel is updated for every frame based on the signal level of the pixel of interest.
Since the SSC is a one-dimensional X-ray camera, we employ the spatial resolving power of the CCD only for the serial direction. Thus, we operate CCD in the parallel summing mode (same as the fast mode in the SIS). The vertical axis of the CCD corresponds to the time sequence. The binning number can be selected as $2^n$ ($n=2$ to $8$). 16 CCD chips in one camera are read cyclically through a multiplexer. We can also operate CCDs in a full-frame mode for a diagnostic mode.

2.4 SS CC

We install a passive radiator panel and a loop heat pipe (LHP) to cool the SSCU. Two radiators are attached to MAXI. The LHP can function as a heat switch and select the radiator panel depending on its temperature.

Due to the limited power consumption, small area of the radiator panel, and the thermal condition around the ISS, we estimate the temperature of the SSCU to be $-70 \sim -30^\circ C$ at the beginning of life (BOL) and $-60 \sim -10^\circ C$ at the end of life (EOL). We therefore install the Peltier cooler to cool down CCD chips. In order to reduce the shock stress during the launch phase, we design the size of the single stage Peltier cooler to be equal to that of a CCD chip. We will perform the acoustic test for MAXI in the end of 2001.

When 1 W is consumed at the Peltier cooler, the difference of temperature between a CCD chip and a base to be $40^\circ C$ and $25^\circ C$ for the base temperature of $-20^\circ C$ and $-60^\circ C$. We thus estimate the the operating temperature of CCD to be $\sim -100 \sim -70^\circ C$ at BOL and $\sim -85 \sim -50^\circ C$ at EOL.

We have constructed the EM of the LHP on which one radiator panel is attached. We perform the test to investigate the thermal performance of LHP for the transient case as well as the steady case.

2.5 CCD

CCD chips used for MAXI are fabricated by Hamamatsu Photonics K.K. (HPK). The CCD chip is three-side buttable with full-frame transfer and has $1024 \times 1024$ pixels of $24\mu m \times 24\mu m$ size with two phase gate structures. The CCD chip is covered by $\sim 2000$Å Al to block optical light.

In order to improve the radiation hardness of CCD, a notch structure is built-in. We also employ the silicon nitride gate since the radiation hardness of the silicon nitride is better than that of silicon oxide (Terry et al. 1983). We have confirmed that these modifications do not aggravate the CCD performance.
For the recovery of the radiation damage, CCD chips possess the charge injection gate at the end of parallel and serial gate structure. We will investigate the radiation hardness of CCD for energetic protons.

We have developed several kinds of CCD chips fabricated both with an epitaxial wafer and with a bulk wafer as shown in Table 1 (Miyaguchi et al. 1999). CCD chips fabricated with epitaxial wafer (epitaxial-1, 2, 3, 4) possess thin depletion layer resulting relatively low dark current. On the other hand, CCD chips fabricated with bulk wafer (bulk-1,2, and 3) possess high dark current and thick depletion layer.

Furthermore, the operating mode of CCD for nominal observation is the parallel-sum mode, which effectively increase the dark current depending on the number of row to be added. We therefore need to develop CCD chips having a low dark current. In order to reduce the dark current for bulk CCD chips, those named bulk-2 and bulk-3 are formed n$^+$ layer on the back surface to absorb electrons produced in the field free region.

3 New CCD Data Acquisition System

Whereas the EM of SSCE function works well, the flexibility is not high enough to tune up the clocking parameters. In order to maximize the X-ray responsivity of the CCD, we need to develop a highly flexible CCD driver. The clock driver circuit employed in the past consists of analog multiplexers, DACs (digital-to-analog converters), and analog amplifiers. DACs determine the clocking voltage whereas analog switches change the timing of clock. For example, two DACs are employed to generate the low and high voltage level of a clock and an analog multiplexer switches each level with a digital signal. This system has been well established but it is not suitable to change the clocking level dynamically.

3.1 Driver System

We have developed a new type of CCD driver system as shown in figure 3. We use one DAC to generate each clock and directly control DACs. In this system, DACs are used to determine both the clocking voltage and its timing. We adopt high-speed optocouplers (HCPL-2430) in order to isolate the ground between the digital part and the analog part. We select TI 8-bit current-output DAC, TLC 7524, whose settling time is $\leq 100$ns. Our design is simple whereas it can produce clocking voltages with a very high flexibility due to its fast settling time.
The new system needs a lot of digital signals because all data bits for all DAC must be controlled simultaneously. For this purpose, we adopted a Field Programmable Gate Array (FPGA). Almost all pins connected to FPGA can be freely configured by user and the exact timing control which is needed for the integration circuit is easily generated. Users can exactly design a specific hardware for a given task without constructing new hardware for each application. We select Altera Flex 10K100E for FPGA. This FPGA device is a static memory type that can be reconfigured simply with the command and has 189 pins available for user. We use VHDL to configure the FPGA. Detailed description of our new driver system is described in Miyata et al. (2001).

3.2 Readout System

We select the integration circuit developed for the EM of SSCE. The digitized CCD video signal is transferred to the VME I/O board possessing the FPGA (Kataoka et al. 1998).

Combining with the new CCD drive system as mentioned in the previous section, the readout noise of our system is $\simeq 3e^{-}$ rms including the readout noise of CCD.

3.3 Determination of Readout Speed

We at first determine the readout speed of CCD. If the readout speed of CCD becomes faster, the dark current can be suppressed but the readout noise becomes larger. These two noise components compensate each other depending on the readout speed.

Figure 4 shows the readout noise as a function of the readout speed. As clearly seen in this figure, the readout noise is constant at the readout speed below 200 kHz. Above 200 kHz, the readout noise becomes worse significantly because the integration time of the CCD video signal is reduced and the intrinsic noise component also increases. We thus select the readout speed to be 125 kHz for a conservative speed.

3.4 X-ray Responsivity of EM CCDs

The X-ray spectrum of $^{55}$Fe obtained with the epitaxial-4 is shown in Figure 5. We accumulated X-ray events having ASCA grades (Yamashita et al. 1997) of 0 (upper) and 0, 2, 3, 4, and 6 (lower). The energy resolution of Mn K$\alpha$ has
a full-width at half-maximum of 135 and 147 eV for grade 0 and grade 0, 2, 3, 4, and 6. We can therefore achieve the comparable X-ray energy resolving power to that of the Astro-E XIS (Hayashida et al. 1998) and the Chandra ACIS (Mark et al. 1999).

The X-ray responsivity for $^{55}$Fe and dark current at $-60^\circ$C for all prototype CCD chips are shown in Table 1. Since improvements are significant both for epitaxial wafer and for the processing technology, the thickness of the depletion layer is achieved $\simeq 40 \, \mu m$ and the energy resolution is $140-150$ eV. Note that the thickness of the depletion layer is comparable to those of Astro-E XIS and Chandra ACIS at reduced dark current mode (inferred voltage is similar to those of our experiments; Mark et al. 1999). For the bulk-1 chip, the depletion depth is thick (48$\mu$m) but the energy resolution is worse than those of other CCDs. The dark current for the bulk CCDs having n$^+$ layer on the back side can be suppressed compared with the bulk-1 CCD. We therefore have selected epitaxial-4 or bulk-3 for the flight models and continue to improve their X-ray responsibities.

4 Summary

We have constructed the engineering model of all components of SSC. The performance test of each component is still ongoing and functions properly.

In order to evaluate CCDs for the SSC, we have developed the new CCD data acquisition system, which enables us to change the clock voltage easily and flexibly with driving a fast DAC chips. The readout noise of our system can be achieved $\leq 3$e$^-\,$ rms. We optimize many kinds of CCDs fabricated from different wafers. We can achieve the comparable X-ray energy resolving power as well as high detection efficiency to those of X-ray CCD cameras onboard other satellites.

References


Table 1
Characteristics of prototype CCDs.

<table>
<thead>
<tr>
<th>wafer</th>
<th>Q.E. $^a$</th>
<th>Depth $^b$</th>
<th>$\Delta E$ $^a$</th>
<th>Dark Current at $-60^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[%]</td>
<td>[µm]</td>
<td>[eV]</td>
<td>[e$^-$ pixel$^{-1}$ s$^{-1}$]</td>
</tr>
<tr>
<td>epitaxial-1</td>
<td>12 ± 0.7</td>
<td>4</td>
<td>142 ± 5.8</td>
<td>7.9 × 10$^{-1}$</td>
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<tr>
<td>epitaxial-2</td>
<td>37 ± 0.8</td>
<td>14</td>
<td>152 ± 3.1</td>
<td>1.5 × 10$^{-1}$</td>
</tr>
<tr>
<td>epitaxial-3</td>
<td>56 ± 1.0</td>
<td>25</td>
<td>143 ± 2.2</td>
<td>5.2 × 10$^{-1}$</td>
</tr>
<tr>
<td>epitaxial-4</td>
<td>73 ± 1.5</td>
<td>42</td>
<td>143 ± 1.9</td>
<td>4.4 × 10$^{-1}$</td>
</tr>
<tr>
<td>bulk-1</td>
<td>79 ± 1.6</td>
<td>48</td>
<td>208 ± 4.7</td>
<td>6.0 × 10$^{-1}$</td>
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<tr>
<td>bulk-2</td>
<td>57 ± 1.2</td>
<td>27</td>
<td>147 ± 3.2</td>
<td>4.0 × 10$^{-1}$</td>
</tr>
<tr>
<td>bulk-3</td>
<td>71 ± 1.5</td>
<td>40</td>
<td>162 ± 2.5</td>
<td>1.6 × 10$^{-1}$</td>
</tr>
</tbody>
</table>

$^a$ Q.E. is a quantum efficiency at 5.9 keV and $\Delta E$ is a FWHM energy resolution at 5.9 keV for ASCA grades of 0, 2, 3, 4, and 6.

$^b$ Depth of the depletion layer and measured at vertical voltage of 4V.
Fig. 1. Block diagram of SSC.
Fig. 2. EM of SSCU with the entrance window (a), and without the entrance window (b). Since the collimator is not installed, CCD chips are seen at the bottom of SSCU. There are two cables connected to the Peltier cooler (c).
Fig. 3. Schematic diagram of the new CCD data acquisition system.
Fig. 4. Readout noise as a function of a readout speed.
Fig. 5. The X-ray spectrum of $^{55}$Fe obtained with the bulk-2. ASCA grades of 0 (upper) and 0, 2, 3, 4, and 6 (lower) are accumulated.